About College

Thiagarajar College of Engineering (TCE), Madurai, an autonomous institution affiliated to Anna University, is one among the several educational and philanthropic institutions founded by the philanthropist andindustrialist Late. Shri. Karumuttu Thiagarajan Chettiar.

- TCE was established in the year 1957.
- TCE is funded by Central and State governments and the Management.
- The Programmes in TCE are approved by AICTE and granted autonomy in 1987.
- TCE has been accredited by NAAC with A+ grade and has secured 64th rank in NIRF 2020.
- TCE offers nine UG programmes, nine PG programmes, and 5 years integrated MSc Data Science.

About Department

The Department of Electronics and Communication Engineering started in the year 1978 with the vision "To empower the Electronics and Communication Engineering students with technological excellence, professional commitment and social responsibility".

- DST-FIST Supported Department, TIFAC CORE on Wireless Technologies.
- Govt. and Industry Sponsored Projects from DRDO, DRDL, DIT, CDAC, ISRO, RCI, NPMASS, AICTE,DST,UGC.
- Established industry supported laboratories from Agilent, Free scale, Altera, CISCO and National Instruments.
- Granted Indian and US patents in the areas of RF, Dental image analysis, Image Analysis and sensors.

Scope and objectives of the FDP

The aim of this programme is to provide participants a complete understanding on UVM testing, an experience on self checking UVM test benches, and to make them proficient at UVM verification. At the end of this programme, the participants will be able to understand the basic concepts of UVM, build actual verification components, build actual verification components, code test benches using UVM, and understand advanced peripheral bus testbenches. Participants will also be able to create and configure reusable, scalable, and robust UVM verification components (UVCs), and UVM testbench structure using the UVM library base classes.

Contents of the FDP

INTRODUCTION

- The Typical UVM Testbench Architecture.
- The UVM Class Library Transaction –level Modeling (TLM).

DEVELOPING REUSABLE VERIFICATION COMPONENTS

- Modeling data items for generation
- Transaction level Components
- Creating the driver and sequencer
- Connecting the driver and sequencer
- Creating the monitor
- Instantiating Components
- Creating the Agent and the Environment
- Enabling Scenario Creation
- Managing of Test-Implementing Checks and Coverage

A Two-Day Faculty Development Program on

"VLSI Design – Universal Design Methodology (UVM)"

23rd & 24th, Sep 2022

Organized by

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

THIAGARAJAR COLLEGE OF ENGINEERING

MADURAI- 625 015

Course Coordinators

Dr.S.Rajaram, Prof & Head

Dr.N.B.Balamurugan, Professor

Dr.D.Gracia Nirmala Rani, Asso. Prof

Dr.V.R.Venkatasubramani, Asst.Prof

UVM USING VERIFICATION COMPONENTS

- Creating a Top-Level Environment
- Instantiating Verification Components
- Creating Test Classes
- Verification Component Configuration
- Creating and Selecting a User-Defined Test
- Creating Meaningful Tests
- Virtual Sequences Checking for DUT Correctness
- Scoreboards Implementing a Coverage Model

UVM USING THE REGISTER LAYER CLASSES

- Using The Register Layer Classes
- Back-Door Access
- Special Registers
- Integrating a Register Model in a Verification Environment
- Integrating a Register Model
- Randomizing Field Values
- PreDefined Sequences

ASSIGNMENT IN TESTBENCHES

- Assignment, APB: Protocol
- Test bench Architecture
- Driver and Sequencer
- Monitor, Agent and Env
- Creating Sequences
- Building Test
- Design and Testing of Top Module

HANDS-ON TRAINING

- To simulate UVM testbench
- Examining the UVM testbench
- Design and simulate sequence items and sequence
- Design and simulate a UVM driver and sequencer
- Design and simulate UVM Monitor and Agent
- Design and simulate a UVM scoreboard and environment, and verifying the outputs of a (faulty) DUT.

Participants

The workshop is open to Faculty of Engineering colleges, Research Scholars and UG/PG Students of Electronics and Communication Engineering. Participants will be expected to have knowledge about VLSI Design.

Registration Fee

The registration fee includes workshop kit, presentation materials, and certificate of participation, and refreshment.

Faculty & Research Scholars	**:**	**Rs.1000/- (Rs.1000+18% GST)**
UG & PG Students	**:**	**Rs.885/- (Rs.750+18% GST)**

Mode of Payment

Participants can pay the registration fee either by a crossed Demand Draft in favor of **The Principal, Thiagarajar College of Engineering** payable at **Madurai** or by using the online link given below.

Online Registration Procedure

Step 1: Make your Registration at https://forms.gle/4sSV6kXFXzuDjc2p8

Step 2: Complete your Payment

i. Click the link given (or) Search https://eazypay.icicibank.com/

ii. Type "T C E" with Space (as mentioned) in the "Enter Institute Name".

iii. Select the Last Option* (“T C E SOUVENIOR “) from the drop-down menu.

iv. Enter the Required Information (Email id, Mobile number, Name, Designation, College Name, Department, FDP Registration Fee).

Step 3: Pay the fees and download the eazypay Transaction Receipt.

Step 4: Update Program Topic Google Form with the Transaction ID and Receipt.

Step 5: Submit Google Form.

Important Dates

Last date for Registration : 15.9.2022

Speakers of the FDP

Resource persons from Industries and Higher learning institutions will deliver the course contents.

Contact Details

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