

THIAGARAJAR COLLEGE OF ENGINEERING, MADURAI-15

(A Govt. Aided Autonomous Institution affiliated to Anna University)

- where Quality and Ethics matter



QEEE COURSES

MEMORY AND IO - ADVANCED COMPUTER ARCHITECTURE

COURSE CONTENT:

Memory subsystem: Main memory organization. RAM structure. Main memory and performance – Memory technology. Types of storage devices. The memory module and its interface. Memory interleaving. Memory hierarchy - operation of memory hierarchy

Cache: Mapping function – Associative, direct and block set-associative. Cache Replacement policies. Cache read and write policies. Cache fetch policies. Unified and split cache. Cache coherence protocol – MESI. Cache performance- Average Memory Access Time, Reducing cache miss penalty and miss rate – Reducing hit time. Example memory hierarchy: ARM processor.

Virtual memory: memory management- paged memory and segmented memory. Main Memory management policies- placement, replacement, fetch and secondary memory update policies. Address translation - TLB design, implementation

I/O subsystem: I/O bus structures. Programmed I/O. I/O interrupts – Interrupt hardware and software, interrupt priority. Direct Memory Access (DMA). I/O data format change and error control. RAID – Reliability, availability and dependability. I/O performance measures – Designing an I/O system